[This question paper contains 4 printed pages.]

Sr. No. of Question Paper: 842

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Your Roll No.

Unique Paper Code

: 234203

Name of the Course

: B.Sc. (H) Computer Science

Name of the Paper

: Computer System Architecture (CSHT-204)

Semester

: II

Duration: 3 Hours

Maximum Marks: 75

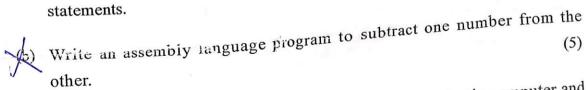
Instructions for Candidates

Write your Roll No. on the top immediately on receipt of this question paper. 1.

- Attempt all questions from Section A. 2.
- Attempt any four questions from Section B. 3.
- Attempt all parts of a question at one place. 4.

SECTION - A

(a) Define fetch, decode and execute phases of the instruction cycle in a basic computer. State the sequence of microoperations using register transfer statements.



- Draw the diagram of the micro-program sequencer of a basic computer and explain its working.
- Convert the following arithmetic expressions from infix to Reverse Polish Notation (RPN):
 - (i) A+B*C+D*E+F

") A+	D+-				
(4) A+]	0710	1*			
	T,	J.	+D1	_	

(5)

(e) The time delay of four segments in a pipeline are as follows:

time $t_1 = 50 \text{ ns}$, $t_2 = 30 \text{ ns}$, $t_3 = 95 \text{ ns}$ and $t_4 = 45 \text{ ns}$. The interface registers delay pipeling 2. time $t_R = 5$ ns. H_{0W} long would it take to add 100 pairs of numbers in the spead task. Determine pipeline? A non pipeline system takes $t_N = 90$ ns to process a task. Determine (5)

the speedup ratio of the pipeline for 100 tasks.

Differentiate between isolated and memory mapped I/O. Give advantages

(5)

(6)

Differentiate between isolated and memory mapped I/O. Give advantages

(6)

(7) (g) Explain direct mapping in cache memory with the help of an example. Draw (5)

SECTION — In SECTION — In Occur in memory and CPU register— I see the occurrence of the section Occur in memory and CpU registers before and after the occurrence of the (5)

Show the contents (in hexadecimal) of registers PC, AR, DR. IR and SC of The initial and ISZ in the memory and address. the basic computer when an ISZ instruction is fetched from the memory and of memory at address executed. The initial content of pC is 7FF. The content of memory at address at address in the initial content of pC is 7FF. The content of memory at address in the content of the Of memory at address C35 is proper at address A9F is OC35. The content of registers in a stants of registers in a stants of registers in a stants of registers in a stants. of memory at address C35 is FFFF. Show the contents of registers in a (5)

What are the characteristics of I/O channels? Draw and explain Multiplexof (5) Let the address stored in the program counter be X1. The two word tex registe execute the instruction is stored in the program counter be X1. The two works stored in X1 has an address part X2. The operand needed to index register

execute the instruction is stored in the program counter be X1. The stored in the many An index register

contains X4. Calculate the effective address of the operand if the addressing mode of the instruction is:

- (i) immediate
- (ii) direct
- (iii) indirect
- (iv) relative

(5) (v) indexed

- 4. (a) Write a symbolic micro program for fetching and execution of an EXCHANGE instruction.
 - (b) A digital computer has a memory unit with a capacity of 16, 384 words of 40 bits each. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no mode bit present). Two instructions are packed in one memory word and a 40 bit Instruction Register (IR) is available in the CPU. Formulate a procedure for fetching and executing an instruction for this computer.
- (a) Draw a six-segment pipeline and its timing diagram for an instruction cycle. Assume that the 3rd instruction is a branch instruction.
 - (b) Write two assembly programs to evaluate the expression X = (A + B) * (C+D)using three and two address instructions respectively.
- 6. (a) List the elements of bus design. Differentiate between synchronous and asynchronous timing with the help of diagrams.
 - (b) Draw the diagram of a DMA module and explain its functions. (5)
- (5) 7. (a) Explain the working of PCI bus in a typical desktop system.

(b) A two way set associative memory uses blocks of four words. The cache can accommodate a true memory uses blocks of four words. can accommodate a total of 2048 words from the main memory. The main memory has a size of 1000 memory has a size of 128K × 32 bits. Design the cache structure and explain how the CPIL (5) explain how the CPU generated address is interpreted. (5)